REMARKS

I. Formal Matters

A. Priority

Applicant thanks the Examiner for acknowledging the claim to foreign priority and for confirming that the certified copy of the priority document was received.

B. Information Disclosure Statement

Applicant thanks the Examiner for initialing the references listed on two form PTO-1449's submitted with the Information Disclosure Statement filed on October 26, 1999. However, the Examiner has not considered references 5-8 submitted in the Information Disclosure Statement filed October 26, 1999, for the reasons set forth at page two of the Office Action. Applicant submits herewith English Abstracts for JP 8-6865, JP 10-161942, JP 10-254694 and JP 6-274409. Accordingly, Applicant respectfully requests that the Examiner initial these references listed on form PTO-1449 and re-submit initialed form PTO-1449 with the next Office paper.

C. Drawings

Applicant submits herewith a proposed drawing correction for Figure 5 and respectfully requests that the Examiner indicate his approval in the next Office paper.

II. Claim Rejections under 35 U.S.C. § 112, second paragraph

Claims 1-7 are rejected under 35 U.S.C. § 112, second paragraph. The claims have been amended to overcome this rejection. Specifically, the language relating to the stages being "good or bad" has been removed. The Examiner is respectfully requested to reconsider and withdraw this rejection in view of the claim amendments.

III. Claim Rejections under 35 U.S.C. § 103

A. The Examiner has rejected claims 1, 3 and 7 under 35 U.S.C. § 103(a) as being unpatentable over Atsumi et al. (U.S. Patent No. 6,160,738).

Claims 1, 3 and 7 each define a new and unobvious combination which forms a computer having unique rewriting capabilities. Included among the features of this new computer is a controller, which among other features, updates a flag area upon determining that one or more stages of a rewriting process has completed. Applicants submit that the claimed combination is neither taught nor suggested by Atsumi.

In contrast, Atsumi teaches a system which updates a flag cell value only after both an erasing step and refreshing step are completed. In addition, since Atsumi does not even determine the completion of one or more stages of the rewriting process, it cannot update a flag cell after the completion of stages of the rewriting process as set forth in claims.

The Examiner points to column 14, line 64 through column 15, line 9, for the teaching of determining completion of stages of the rewriting processing and recording results of the determination into respective flag areas. The Examiner is in error. The cited section discloses reading a status value of the flag cells, and performing a refresh operation in response to a flag

cell containing a second logical level. The refresh operation then refreshes the contents of the memory cells of the corresponding refresh block and subsequently updates the value of the corresponding flag cell.

The refresh operation of Atsumi consists of reading data out of a memory cell and programming it thereto again. (Col. 5, lines 1-2). After an erasing step is completed, the refresh operation begins. (Col. 4, lines 50-52). Subsequent to completion of the refresh operation, the flag cell value is updated to reflect the new status. (Col. 2, lines 34-36). Thus, while Atsumi discloses updating a flag cell value after the rewriting process is complete, Atsumi does not determine the completion of stages of the rewriting processing, whereby the results are subsequently recorded into respective flag areas.

In view of at least the foregoing distinctions, Applicant respectfully submits that claims 1, 3 and 7 are allowable over the applied art, and the Examiner is kindly requested to reconsider and allow the claims.

B. Claims 2 and 5 stand rejected as being unpatentable over Atsumi et al. in view of Sukegawa et al. (U.S. Patent No. 5,603,001). Claim 2 depends from independent claim 1 and claim 5 depends from independent claim 3. Applicants submit that the above deficiencies regarding Atsumi are not overcome by Sukegawa. Therefore, claims 2 and 5 are in condition for allowance at least by virtue of their dependency.

IV. Allowable Subject Matter

Applicant thanks the Examiner for indicating that claims 4 and 6 would be allowable if rewritten to overcome the rejections under §112, second paragraph. Accordingly, because the rejections under §112, paragraph 2 are believed to have been overcome as noted above, claims 4 and 6 should now be allowed.

V. New Claims

For additional claim coverage merited by the scope of the invention, Applicants are adding new claims 8-30. For at least the reasons set forth above in regard to independent claims 1, 3, 4 and 7, it is believed that new dependent claims 8-30 are also patentable over the cited prior art references.

VI. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Submitted herewith is a Petition For Extension Of Time with fee and an Excess Claim Fee Calculation Letter with fee.

Applicant hereby petitions for any extension of time which may be required to maintain the pendency of this case, and any required fee, except for the Issue Fee, for such extension is to be charged to Deposit Account No. 19-4880.

Respectfully submitted,

Kenneth Fields

Kenneth W. Fields
Registration No. P-52,430

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims are amended as follows:

Claim 1. (Amended) A computer [microcomputer] provided with a [flash] memory and having a self-programming function of rewriting a program stored in said [flash] memory, comprising:

a rewrite program area for storing a program for a rewriting processing procedure for said [flash] memory; and

a controller for forming a plurality of flag areas locally in said [flash] memory when the rewriting program [stored in external storage means or said rewrite program area] is written into said [flash] memory, performing determination of completion of [a plurality of] one or more stages of rewriting processing [or determination of whether the plurality of stages are good or bad] and recording results of the determination into the respective flag areas.

Claim 2. (Amended) A computer [microcomputer] provided with a [flash] memory according to claim 1, wherein said [flash] memory includes a plurality of blocks each of which is an erasable unit and includes a data area and a flag area, and said controller maps the data areas of the plurality of blocks to successive addresses.

Claim 3. (Amended) A computer [microcomputer] provided with a [flash] memory and having a self-programming function of rewriting a program stored in said [flash] memory, comprising:

a rewrite program area for storing a program for a rewriting processing procedure for said [flash] memory;

rewriting means for forming a plurality of flag areas locally in said [flash] memory when the rewriting program [stored in external storage means or said rewrite program area] is written into said [flash] memory; and

a controller for performing determination of completion of [a plurality of] one or more stages of rewriting processing [or determination of whether the plurality of stages are good or bad] and recording results of the determination into the respective flag areas through said rewriting means.

Claim 4. (Amended) A computer [microcomputer] provided with a [flash] memory and having a self-programming function of rewriting a program stored in said [flash] memory, comprising:

a rewrite program area for storing a program for a rewriting processing procedure for said [flash] memory;

rewriting means for forming a plurality of flag areas locally in said [flash] memory when the rewriting program [stored in external storage means or said rewrite program area] is written into said [flash] memory;

a controller for performing determination of completion of [a plurality of] one or more stages of rewriting processing [or determination of whether the plurality of stages are good or bad] and recording results of the determination into the respective flag areas through said rewriting means; and

flag state notification means for comparing, when power supply is made available after the rewriting is completed, values read out from said flag areas with expected values for said flag areas stored in advance and notifying said controller of results of the comparison.

Claim 5. (Amended) A computer [microcomputer] provided with a [flash] memory according to claim 3, wherein said [flash] memory includes a plurality of blocks each of which is an erasable unit and includes a data area and a flag area, and said rewriting means maps the data areas of the plurality of blocks to successive addresses.

Claim 6. (Amended) A computer [microcomputer] provided with a [flash] memory according to claim 4, wherein said [flash] memory includes a plurality of blocks each of which is an erasable unit and includes a data area and a flag area, and said rewriting means maps the data areas of the plurality of blocks to successive addresses.

Claim 7. (Amended) A method of storing a program into a [flash] memory of a computer [microcomputer] provided with said [flash] memory and having a self-programming function of rewriting the program stored in said [flash] memory, wherein

a plurality of flag areas are formed locally in said [flash] memory when a rewriting program is written into said [flash] memory, and determination of completion of [a plurality of] one or more stages of rewriting processing [or determination of whether the plurality of stages are good or bad] is performed, whereafter results of the determination are recorded into the respective flag areas.

Claims 8-30 are added as new claims.